Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **INPUT**
2. **OUTPUT**
3. **GND**

**.079”**

**.079”**

**MASK**

**REF**

**3**

**1**

**2**

**120-5.0**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: GND = .010” X .022”**

**Backside Potential: INPUT**

**Mask Ref: 120-5.0**

**APPROVED BY: DK DIE SIZE .079” X .079” DATE: 4/27/23**

**MFG: SILICON GENERAL THICKNESS .015” P/N: UA7905**

**DG 10.1.2**

#### Rev B, 7/1